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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 003692.P051 Total Pages 3

First Named Inventor or Application Identifier Balu Balakrishnan

Express Mail Label No. EL639015577US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. XX Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. XX Specification (Total Pages 33)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 4)

4. X Oath or Declaration (Total Pages 5)

a. X Newly Executed (Original or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ____ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ____ Microfiche Computer Program (Appendix)

7. _____ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
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ACCOMPANYING APPLICATION PARTS

8. __X__ Assignment Papers (cover sheet & documents(s))
9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
_____ b. Power of Attorney
10. _____ English Translation Document (if applicable)
11. _____ a. Information Disclosure Statement (IDS)/PTO-1449
_____ b. Copies of IDS Citations
12. _____ Preliminary Amendment
13. __X__ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. _____ a. Small Entity Statement(s)
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17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:
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18. **Correspondence Address**

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6-30-2000
(Date signed)

Serial/Patent No.: **** Filing/Issue Date: Herewith
Client: Power Integrations, Inc.
Title: METHOD AND APPARATUS FOR IMPROVING EFFICIENCY IN A SWITCHING REGULATOR AT LIGHT LOADS
BSTZ File No.: 003692.P051 Atty/Secty Initials: JYG/cab
Date Mailed: June 30, 2000 Docket Due Date: ****

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- ☐ Small Entity Declaration for Indep. Inventor/Small Business
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☐ Other: _____

UNITED STATES PATENT APPLICATION

FOR

METHOD AND APPARATUS FOR IMPROVING EFFICIENCY IN A SWITCHING REGULATOR AT LIGHT LOADS

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METHOD AND APPARATUS FOR IMPROVING EFFICIENCY IN A SWITCHING REGULATOR AT LIGHT LOADS

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to power supplies and, more specifically, the present invention relates to a switching regulator.

Background Information

Electronic devices use power to operate. Switched mode power supplies are commonly used due to their high efficiency and good output regulation to power many of today's electronic devices. In a known switched mode power supply, a low frequency (e.g. 50 or 60 Hz mains frequency), high voltage alternating current (AC) is converted to high frequency (e.g. 30 to 300 kHz) AC, using a switched mode power supply control circuit. This high frequency, high voltage AC is applied to a transformer to transform the voltage, usually to a lower voltage, and to provide safety isolation. The output of the transformer is rectified to provide a regulated DC output, which may be used to power an electronic device. The switched mode power supply control circuit usually provides output regulation by sensing the output and controlling it in a closed loop.

A switched mode power supply may include an integrated circuit switching regulator, which may include an output transistor coupled in series with a primary winding of the transformer. Energy is transferred to a secondary winding of the transformer by turning on and off of the output transistor in a

manner controlled by the switching regulator to provide a clean and steady source of power at the DC output. The transformer of a switched mode power supply may also include another winding called a bias or feedback winding. In some switched mode power supplies, the feedback or control signal can come through an opto-coupler from a sense circuit coupled to the DC output. The feedback control signal may be used to modulate a duty cycle of a switching waveform generated by the switching regulator. The duty cycle is defined as the ratio of the on time to the switching period of the output transistor. If there is a large load at the DC output of the power supply, the switching regulator responds to this situation by increasing the duty cycle and thereby delivering more power to the load. If the load becomes lighter, then the switching regulator senses this change through the feedback signal and reduces the duty cycle.

If the load is further reduced and if the power delivered to the DC output cannot be reduced indefinitely, then the DC output voltage increases, resulting in poor output regulation. This unfavorable situation becomes worse if the load is completely removed. To improve the output regulation, a constant load may be connected internal to the power supply. However, because the internal load is always connected, even when there is no load at the DC output, the power supply efficiency is decreased. The power supply efficiency loss is generally due to three components: (1) DC operating power that keeps the switching regulator circuitry operating, (2) the switching losses that are due to switching of the switching regulator output transistor and its drivers--switching losses are directly

proportional to the operating frequency, and (3) the power that is consumed by the internal load.

In order to improve efficiency, a switching regulator may use a method called cycle skipping. Cycle skipping method involves reducing the duty cycle as the load decreases, and when the duty cycle is reduced down to a predetermined minimum duty cycle, it alternatively switches for some duration of time and stays idle for another duration of time depending on the load. During this mode, if the load increases very slightly, the output transistor will switch at minimum duty cycle for a short time until the power demanded by the load is delivered and then stop switching again. In theory, the cycle skipping mode decreases the switching losses at light loads since switching occurs as intermittent groups of pulses. Also, cycle skipping eliminates the need for the constant internal load. However, if the groups of pulses occur at a frequency that is within the audio range and the minimum duty cycle is larger than optimum, then the power supply may create an undesirable audio noise. In addition, cycle skipping degrades the output ripple since it typically occurs in groups of pulses and therefore the energy is delivered to the load intermittently.

SUMMARY OF THE INVENTION

Switching regulator methods and apparatuses are disclosed. In one embodiment, a switching regulator includes a power switch coupled between first and second terminals. The first terminal is to be coupled to an energy transfer element of a power supply and the second terminal is to be coupled to a supply rail of the power supply. A control circuit is coupled to a third terminal and the power switch. The third terminal is to be coupled to an output of the power supply. The control circuit is coupled to generate a feedback signal responsive to the output of the power supply. The control circuit is coupled to switch the power switch in response to the feedback signal. The control circuit is coupled to switch the power switch at a fixed switching frequency for a first range of feedback signal values and coupled to vary a switching frequency of the power switch without skipping cycles in response to the feedback signal for a second range of feedback signal values. Additional features and benefits of the present invention will become apparent from the detailed description, figures and claims set forth below.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention detailed illustrated by way of example and not limitation in the accompanying figures.

Figure 1 is a schematic illustrating one embodiment of a power supply including a switching regulator in accordance with the teachings of the present invention.

Figure 2 is a schematic illustrating one embodiment of a switching regulator in accordance with the teachings of the present invention.

Figure 3 is a timing diagram illustrating waveforms of one embodiment of switching regulator operating at full frequency in accordance with the teachings of the present invention.

Figure 4 is a timing diagram illustrating waveforms of one embodiment of switching regulator operating at a lower frequency in accordance with the teachings of the present invention.

Figure 5 is a diagram illustrating one embodiment of a relationship between frequency and current in one embodiment of switching regulator in accordance with the teachings of the present invention.

Figure 6 is a diagram illustrating one embodiment of a relationship between duty cycle and current in one embodiment of switching regulator in accordance with the teachings of the present invention.

DETAILED DESCRIPTION

Method and an apparatus for regulating a power supply are disclosed. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one having ordinary skill in the art that the specific detail need not be employed to practice the present invention. In other instances, well-known materials or methods have not been described in detail in order to avoid obscuring the present invention.

The present invention improves the efficiency of a power supply switching regulator with pulse width modulation by decreasing the operating frequency at light loads. Switching losses are decreased with one embodiment of the present invention since switching losses are directly proportional to operating frequency. Audio noise problems associated with present day switching regulators are no longer a problem because the minimum operating frequency of a switching regulator in accordance with the teachings of the present invention is chosen to be above audible frequency. One embodiment of the present invention also improves output ripple since the pulse width modulation is continuous in nature and not intermittent.

To illustrate, Figure 1 is a block diagram showing a power supply 101 including one embodiment of a switching regulator 139 in accordance with the teachings of the present invention. As shown, a bridge rectifier 105 and capacitor 107 are coupled to rectify and filter an input alternating current (AC) voltage

received at AC mains 103. In one embodiment, a positive power supply rail 108 and a ground power supply rail 106 are provided across capacitor 107. The rectified voltage generated by bridge rectifier 105 and capacitor 107 is received at a primary winding 115 of an energy transfer element, such as transformer 113. In one embodiment, transformer 113 includes a secondary winding 117 and a bias winding 119. Diode 121 and capacitor 123 rectify and filter DC output 129, whereas diode 125 and capacitor 127 rectify and filter the bias winding.

The switching regulator 139 includes a drain terminal 141 coupled to the primary winding 115 and a source terminal 143 coupled to the ground rail 106. In one embodiment, switching regulator 139 includes a control circuit 149, which generates a drive signal 161 to switch a power switch 147 to transfer the energy to the secondary winding 117 using transformer 113. Diode 111 and Zener 109 are used for clamping the drain terminal 141.

A load 130 is configured to be coupled across output 129. A feedback loop is formed from output 129 through output sense circuit 131 to a control terminal 145 of the switching regulator 139. The feedback loop includes the output sense circuit 131 and opto-coupler 133. The opto-coupler 133 includes a transistor 135 that is optically coupled to a photodiode 137. An output sense signal 146 responsive to output sense circuit 131 is coupled to be received by control terminal 145 of the switching regulator 139. Output sense signal 146 may be a current or a voltage. The combined bias supply current as well as the feedback current is provided to the control terminal 145 by the opto-coupler 133

using the bias winding 119. Thus, the control terminal 145 may be characterized as a supply voltage (V_S)/feedback terminal for switching regulator 139. This control terminal 145 is therefore frequently referred to as a combined electrical terminal. An external capacitor 151 is connected between control terminal 145 and ground.

Figure 2 is a schematic illustrating one embodiment of a switching regulator 239 in accordance with the teachings of the present invention. In one embodiment, switching regulator 239 of Figure 2 may be utilized in place of switching regulator 139 of Figure 1. As shown, an example embodiment of switching regulator 239 includes a power switch 247 coupled between a drain terminal 241 and a source terminal 243. A gate of power switch 247 is coupled to be switched in response to a drive signal 261 generated by control circuit 249.

Control circuit 249 includes a feedback signal circuit 349 coupled to generate a feedback signal 248 responsive to an output sense signal 246 coupled to be received by control terminal 245. In one embodiment, an internal bias current for switching regulator 239 during normal operation is provided by an internal shunt regulator coupled to control terminal 245. In one embodiment, an external capacitor, such as capacitor 151 of Figure 1, is coupled to control terminal 245. For instance, one embodiment of switching regulator 239 is powered after an initial turn-on by current into control terminal 245 through opto-coupler 133 from output sense circuit 131, which is coupled to the output 129 of power supply 101, as shown in Figure 1. Part of the current that goes into control

terminal 245 powers up the circuitry of switching regulator 239 and the remainder is shunted to ground by the shunt regulator. Feedback signal 248 is extracted from the amount of current that is shunted to ground. If there is a substantial load 130 coupled to the output 129 of power supply 101, then all available current goes to the load.

To illustrate, attention is directed to feedback signal circuit 349 of Figure 2. As shown, comparator 456 includes a positive terminal coupled to an internal reference voltage. The negative terminal of comparator 456 is connected to a voltage that is a fraction of the control terminal 245 voltage through a voltage divider network of resistors including resistors 202 and 203. Comparator 456 compares the internal reference voltage to the fraction of control terminal 245 voltage. If the internal reference voltage is lower than the fraction of control terminal 245 voltage, indicating that the control terminal 245 voltage is at the nominal voltage, the output of comparator 456 goes low, turning on transistor 204. Any excess current that is going into the control terminal 245 is shunted to ground through transistors 204 and 205. Since the transistors 205 and 207 form a current mirror, a proportional fraction of this shunt current is used as the feedback current in transistor 207. The feedback current is converted to a feedback voltage signal through resistor 206, from which feedback signal 248 is generated.

An example embodiment of control circuit 249 includes a pulse width modulator (PWM) circuit 348. PWM circuit 348 generates drive signal 261 in response to feedback signal 248, which is used to control the duty cycle of power

switch 247. PWM circuit 348 includes an oscillator 449 that generates three signals: SAW 451, CLOCK 453 and DMAX 455. As illustrated, the DMAX 455 signal is high during the ramp-up of SAW 451 and DMAX 455 is low during the ramp-down of SAW 451. In one embodiment, the CLOCK 453 signal is a short pulse generated at the low to high transition of DMAX 455. The CLOCK 453 signal is coupled to the S input of flip-flop 463 to set flip-flop 463.

When the CLOCK 453 signal goes high, the Q signal output of the flip-flop 463 goes high and remains high until the flip-flop 463 is reset by the R input of flip-flop 463 going high at a later time. The Q signal output of flip-flop 463 is coupled to one of the inputs of the NAND gate 465. The other input of the NAND gate 465 comes from the DMAX 455 signal of the oscillator 449. Since DMAX 455 is also high during this time, the output of NAND gate 465 is low and the output of the inverter 469 is high. In one embodiment, the output of inverter 469 is drive signal 261 coupled to switch power switch 247.

When drive signal 261 is high, the power switch 247 is on. In one embodiment, drive signal 261 is coupled to turn off power switch 247 when either of the following conditions are met: the reset R input of the flip-flop 463 goes high, or, DMAX 455 of oscillator 449 goes low, which corresponds to maximum duty cycle condition during start-up or an overload condition. The reset R input of the flip-flop 463 goes high if the output of the comparator 457 goes high, or, if the current limit signal input of OR gate 458 goes high.

As shown, one input of OR gate 458 is coupled to receive the current limit signal and the other input of OR gate 458 is coupled to receive an output of comparator 457. In one embodiment, the current limit signal going high indicates that the current through the power switch 247 has exceeded a prescribed limit and the power switch 247 is immediately turned off. The output of comparator 457 goes high when the SAW 451 signal of oscillator 449 is higher than the feedback signal 248 coming from the drain of transistor 207. In one embodiment, the feedback signal 248 is a very slow moving signal--almost a DC level signal in comparison to the SAW 451 signal of oscillator 449. In one embodiment, the SAW 451 signal is a 100 kHz saw-tooth signal.

In one embodiment, PWM circuit 348 operates under at least three different conditions: (1) when the feedback signal 248 is less than the "valleys" of the SAW 451 signal, (2) when the feedback signal 248 is greater than the "peaks" of the SAW 451 signal, and (3) when the feedback signal 248 is in between the "peaks" and "valleys" of the SAW 451 signal.

When there is a considerable current through the resistor 206, there is a corresponding voltage drop across resistor 206 and feedback signal 248 is below the "valleys" of the SAW 451 signal. In one embodiment, a large amount of current through the resistor 206 indicates that there is large amount of current being dumped into the control terminal 246, which in turn indicates that the power demand by load 130, which is coupled to the output 129 of power supply 101, is low. In this situation, the positive terminal of the comparator 457 is always

greater than the negative terminal and the output of the comparator 457 is always high, which keeps the R input of flip-flop 463 high through OR gate 458. When CLOCK 453 signal sets the flip-flop 463 through the S input, the Q output of flip-flop 463 is ready to go high and pull the gate of power switch 473 high to turn on power switch 473. However, since R input of the flip-flop 463 is kept high, the flip-flop 463 is reset immediately and the Q output of flip-flop 463 goes back down immediately, never allowing the power switch 247 to turn on.

In one embodiment, the feedback signal 248 is greater than the "peaks" of the SAW 451 signal when there is not enough current through the resistor 206 to drop the voltage of feedback signal 248 down. In one embodiment, this is the case when the output 129 is heavily loaded by load 130. In this situation, the positive terminal of the comparator 457 is always less than the negative terminal and the output of the comparator 457 is always low, keeping the R input of flip-flop 463 low and never resetting the flip-flop 463. This means that after the CLOCK 453 signal turns on the power switch 473 by setting the flip-flop 463, which makes the Q output of flip-flop 463 go high, the power switch 247 is not turned off until the DMAX 455 signal goes from high to low, or until the power switch 247 reaches current limit, allowing the output transistor to remain on for the maximum duty cycle or until power switch 247 reaches its current limit.

In one embodiment, when the feedback signal is less than the "peaks," but greater than the "valleys" of the SAW 451 signal, the power supply 101 is operating within its nominal load range. In this case, PWM 348 will set the

proper duty cycle for drive signal 261 in response to feedback signal 248 to keep the output 129 of power supply 101 regulated.

In one embodiment, control circuit 249 also includes a timer circuit 347 in accordance with the teachings of the present invention. In one embodiment, if the duty cycle of drive signal 261 is larger than 10%, the switching regulator 239 operates at a full frequency. In one embodiment, the full frequency is 100 kHz. It is appreciated of course that actual values provided in this disclosure, such as the 100 kHz frequency value, are provided for explanation purposes and that other actual values may be utilized in accordance with the teachings of the present invention. For purposes of this disclosure, the duty cycle of drive signal 261 is equal to the on-time of drive signal 261 divided by the period T of drive signal 261. The period T is equal to the on-time + off-time of drive signal 261. Thus, for a drive signal 261 with a full frequency of 100 kHz, the period T of each cycle of drive signal 261 is equal to 1/100 kHz or 10 μs and the on-time of a 10% duty cycle signal is equal to 1 μs. Thus, the off-time of a 10% duty cycle signal is equal to 10 μs - 1 μs, or 9 μs. It is appreciated that PWM circuit 348 adjusts the duty cycle of drive signal 261 in response feedback signal 248, which is responsive to the level of the load 130 coupled to output 129 as well as the input voltage of power supply 101.

In one embodiment, there are two modes of operation for a switching regulator 239 in accordance with the teachings of the present invention--full frequency and low frequency. In one embodiment, the on-time of the power

switch 247, which is responsive to feedback signal 248, determines whether switching regulator 239 operates at full frequency or low frequency. In one embodiment, when the on-time of drive signal 261 is greater than 1 μs, the PWM circuit 348 operates in full frequency mode. When the on-time of drive signal 261 is less than 1 μs, the PWM circuit 348 operates in low frequency mode. Therefore, since the duty cycle of drive signal 261 is responsive to feedback signal 248, the PWM circuit 348 operates in full frequency mode for one range of values for feedback signal 248 and PWM circuit 348 operates in low frequency mode for another range of values for feedback signal 248.

In one embodiment, switching regulator 239 is operated in full and low frequency modes as follows. A signal designated TMIN 257 is derived from the DMAX 455 signal. In one embodiment, TMIN 257 includes a pulse that is generated at each rising edge of DMAX 455. As illustrated, the duration of the pulse of TMIN 257 is determined by a capacitor 353 and current sources 351 and 352. In one embodiment, capacitor 353 is coupled to be discharged through current sources 351 and 352 through transistor 210. In one embodiment, current source 351 draws charge at a rate 30 times greater than current source 352 from capacitor 353. When both current sources 351 and 352 are on at the same time to discharge capacitor 353, the duration of the TMIN 257 pulse width will be 1 μs, 10% of the full frequency period of one embodiment of drive signal 261. In one embodiment, the current source 352 is always activated to discharge capacitor 353. However, the current source 351 is only activated to discharge capacitor 353

when the output of inverter 479 is high, or output of AND gate 478 is low. In one embodiment, AND gate 478 output will always be low if the gate of power switch 247 is on for longer than 1 μs since AND gate 478 combines an inverted drive signal 261 (from the output of NAND gate 465) with TMIN 257. In one embodiment, when the drive signal 261 is on for longer than 1 μs, the AND gate 478 output remains low and transistor 201 remains on to keep oscillator 449 unaffected. In one embodiment, the frequency of drive signal 261 remains constant at 100 kHz in this case.

In one embodiment, as the duty cycle of drive signal 261 falls below 10% in response to feedback signal 248, the switching regulator 239 goes into low frequency operation. In one embodiment, as the duty cycle of drive signal 261 drops below 10%, or the on-time of drive signal 261 falls below 1 μs, the output of the NAND gate 465 goes high while TMIN 257 is still high. During this time, if the status of drive signal 261 was determined through the feedback signal 248, instead of the current limit signal received at the input of OR gate 458, the output of the comparator 456 is also high. With all of the inputs of AND gate 478 being high, the output of AND gate 478 goes high and turns off transistor 201, cutting off the current into the oscillator 449 and suspending oscillations generated by oscillator 449.

In one embodiment, oscillator 449 maintains the value of SAW 451 at its last voltage magnitude, and the signals CLOCK 453 and DMAX 455 stop switching in response to oscillator 449 being suspended in response to transistor

201 being turned off. In one embodiment, when the output of AND gate 478 goes high, the output of inverter 479 goes low and transistor 208 turns off, which deactivates the current source 351 from discharging capacitor 353. Since the current that discharges the capacitor 353 is 31 times smaller now that current source 351 deactivated, capacitor 353 discharges at a slower rate and remains charged for a longer amount of time. Consequently, the remaining on-time of TMIN 257 is increased by 31 times. As a result, the pulse width of TMIN 257 is increased from a fixed 1 μs value to the value determined by the following equation:

For DSPW > 1μs: TMINPW = 1 μs;

for DSPW < 1μs: TMINPW = ((1 μs - DSPW) * 31) + DSPW (Eq. 1)

where TMINPW is TMIN 257 pulse width and DSPW is drive signal 261 pulse width.

The oscillator 449 is suspended from switching for the duration of TMIN 257 pulse width minus the drive signal 261 pulse width and then released. When released, the operation of oscillator 449 resumes from where it left off and SAW 451 signal ramps up from the point at where it had been suspended. Accordingly, the switching period of drive signal 261 is increased from 10 μs of full frequency operation to a value determined by the following equation:

For DSPW < 1μs: LFPDS = (TMINPW – DSPW) + 10 μs (Eq. 2)

where LFPDS is low frequency period of drive signal 261 and TMINPW is TMIN 257 pulse width.

To illustrate, Figures 3 and 4 show full frequency and low frequency operation, respectively, of a switching regulator in accordance with the teachings of the present invention. In particular, Figure 3 shows full frequency operation, which in one embodiment occurs when feedback signal 248 is in a range that causes the duty cycle of drive signal 261 to be greater than 10%. As shown in Figure 3, feedback signal 248 is in between the "peaks" and "valleys" of SAW 251 signal. SAW 251 signal rises in from "valley" to "peak" in 6 μs and falls from "peak" to "valley" in 4 μs, which results in a full operating frequency of 100 kHz. In the example shown, drive signal has an on-time of 2 μs or a duty cycle of 20%, which is greater than 10%. Accordingly, switching regulator 239 operates in full frequency mode. The inverted drive signal 259 keeps both current sources 351 and 352 activated all the time, allowing capacitor 353 to be discharged at the faster rate for an entire 1 μs . Thus, TMIN 257 has a pulse width or on-time of 1 μs.

In comparison, Figure 4 shows low frequency operation, which in one embodiment occurs when feedback signal 248 is in a range that causes the duty cycle of drive signal 261 to be less than 10%. In the particular example illustrated in Figure 4, the on-time of drive signal 261 is only 0.5 μs, which is less than 1 μs. As shown, since the on-time of drive signal 261 is only 0.5 μs, which is less than 1 μs, capacitor 353 is still not fully discharged when current source 351 is deactivated and oscillator 449 is suspended. As shown, SAW 251 signal is caused to be held at the voltage when oscillator 449 was suspended and TMIN 257 now

remains high for more than 1 μs since capacitor 353 is discharged at a slower rate as a result of current source 351 being deactivated. Indeed, as shown, TMIN 257 remains high for the next 0.5 μs * 31 = 15.5 μs. After TMIN 257 goes low, the operation of oscillator 449 is resumed and SAW 251 signal continues to oscillate from where it left off to rise to its "peak" in 5.5 μs and subsequently fell to its "valley" in the normal 4 μs.

In the illustrated example of Figure 4, the switching frequency of drive signal 261 is reduced down to 39.2 kHz and the period of the drive signal has been increased to 25.5 μs (0.5 μs + 15.5 μs + 5.5 μs + 4 μs). If the voltage of feedback signal 248 goes down more, the switching frequency of drive signal 261 decreases further in accordance with the teachings of the present invention. Note that the frequency of drive signal 261 is reduced without skipping cycles of drive signal 261 in accordance with the teachings of the present invention. Instead, the period of each cycle is increased to reduce the frequency of drive signal 261. In one embodiment, both the on-time and the off-time of each cycle of the drive signal 261 are adjusted simultaneously when increasing the period of the drive signal 261 in accordance with the teachings of the present invention.

In one embodiment, the lowest frequency that the power supply controller can go to can be calculated using the formulas above. In particular, assuming that the as the feedback signal 248 voltage decreases down to the voltage of the "valleys" of the SAW 251 signal, the on-time of drive signal 261 reduces to a

substantially zero or negligible amount. In this case, using Equations 1 and 2 above:

$$TMINPW = ((1\ \mu s - \sim 0\ \mu s) * 31) + \sim 0\ \mu s = 31\ \mu s, \quad \text{(Eq.3)}$$

$$LFPDS = (TMINPW - 0\mu s) + 10\ \mu s = 41\ \mu s \quad \text{(Eq. 4)}$$

where TMINPW is TMIN 257pulse width and LFPDS is low frequency period of drive signal 261. Thus, the period of drive signal 261 at the lowest frequency in this particular embodiment is 41 μs.

The low frequency period of 41 μs corresponds to a frequency of 1/41 μs, or 24.4 kHz. Since the lowest switching frequency of 24.4 kHz is higher than the human audible frequency range of 20 to 20 kHz, a power supply 101 regulated with a switching regulator in accordance with the teachings of the present invention will not produce any audible noise, even at its lowest frequency.

Referring back to the embodiment shown in Figure 2, timer circuit 347 also includes a transistor 212 switched in response to the output of AND gate 478. Transistor 212 acts as a switch to allow current to flow through resistor 211. The purpose of resistor 211 and transistor 212 is to keep the current consumption of switching regulator 239 during low frequency operation the same as the current consumption was during full frequency operation. As discussed earlier, one embodiment of switching regulator 239 is powered by a current into the control terminal 245 through opto-coupler 133 from output sense circuit coupled 131 to the output 129 of the power supply 101. In one embodiment, part of the current that goes into the control terminal 245 powers up the circuitry of switching

regulator 239 and the remainder of the current is shunted to ground by the shunt regulator. The feedback signal 248 is extracted from the amount of the current that is shunted to ground.

As the frequency of drive signal 261 decreases during the low frequency operation, the power consumed due to switching of the internal circuitry of switching regulator 239 decreases, resulting in less current going into the circuitry of switching regulator 239 and more current being shunted to ground. As the current being shunted to ground increases, the portion of this current that is being used for extracting the feedback signal 248 would also increase, causing the feedback signal 248 to go lower. Correspondingly, the switching frequency of drive signal 261 would then go lower due to decreased current consumption of the switching regulator 239.

Thus, to keep the current consumption of the switching regulator substantially constant, additional current is drawn in low frequency mode operation through resistor 211 and transistor 212 to compensate for the difference in switching losses between full and low frequency operating modes of switching regulator 239 in accordance with the teachings of the present invention. If the additional current is greater than the reduction of power consumption, then, the pulse width modulation gain, i.e. the duty cycle versus control terminal 245 current, will be slightly reduced.

Figures 5 and 6 are diagrams illustrating the relationships of frequency vs. current 561, and duty cycle vs. current 661, respectively, in one embodiment of

switching regulator in accordance with the teachings of the present invention. In particular, Figure 6 shows that as the current into the control terminal 245 increases, the duty cycle of drive signal 261 decreases. In one embodiment, the duty cycle of drive signal 261 decreases in a linear type fashion relative to the current into control terminal 245 across the full and low frequency modes of the switching regulator in accordance with the teachings of the present invention.

Figure 5 shows that in one embodiment as the duty cycle of drive signal 261 decreases, the switching frequency of drive signal 261 remains fixed until the duty cycle is reduced to a value such as 10%. As the duty cycle of drive signal 261 falls below 10%, in one embodiment, the frequency of drive signal 261 starts to decrease gradually, all the way down to approximately 25 kHz, by which time the duty cycle of drive signal 261 goes down to 0%. In one embodiment, the frequency of drive signal 261 decreases in a nearly linear type fashion in response to control terminal 245 current across the full and low frequency modes of the switching regulator in accordance with the teachings of the present invention.

In one embodiment, feedback signal 248 is responsive to the control terminal 245 current. Therefore, for one range of feedback signal 248 values, the switching regulator 239 operates at a fixed frequency and for another range of feedback signal 248 values, the frequency of operation of the switching regulator 239 is decreased in response to the feedback signal 248. In one embodiment, the boundary of fixed frequency operation and low frequency operation is a feedback signal 248 value that corresponds to a 10% duty cycle.

In one embodiment of the present invention, switching regulator 239 is operated at a full frequency operation at 130 kHz. In this embodiment, the on-time of drive signal 261 that corresponds to the boundary at which switching regulator 239 is operated in either full frequency or low frequency can be adjusted by adjusting the TMIN 257 time constant when both current sources 351 and 352 are on. In one embodiment, the minimum frequency of drive signal 261 is 40 kHz. In another embodiment, switching regulator 239 is operated at a full frequency operation at 65 kHz with a minimum frequency for drive signal of 20 kHz.

In the foregoing detailed description, the method and apparatus of the present invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the present invention. The present specification and figures are accordingly to be regarded as illustrative rather than restrictive.

CLAIMS

What is claimed is:

1. A switching regulator, comprising:

a power switch coupled between first and second terminals, the first terminal to be coupled to an energy transfer element of a power supply and the second terminal to be coupled to a supply rail of the power supply;

a control circuit coupled to a third terminal and the power switch, the third terminal to be coupled to an output of the power supply, the control circuit coupled to generate a feedback signal responsive to the output of the power supply, the control circuit coupled to switch the power switch in response to the feedback signal, the control circuit coupled to switch the power switch at a fixed switching frequency for a first range of feedback signal values, the control circuit coupled to vary a switching frequency of the power switch without skipping cycles in response to the feedback signal for a second range of feedback signal values.

2. The switching regulator of claim 1 wherein the control circuit comprises:

a feedback signal circuit coupled to the third terminal, the feedback signal circuit coupled to generate the feedback signal; and

a pulse width modulator circuit coupled to switch the power switch in response to the feedback signal.

3. The switching regulator of claim 1 wherein the first and second ranges of the feedback signal correspond to first and second ranges of levels of a load coupled to the output of the power supply.

4. The switching regulator of claim 2 wherein the first and second ranges of the feedback signal correspond to first and second ranges of on-time values of a drive signal generated by the pulse width modulator circuit to switch the power switch.

5. The switching regulator of claim 2 wherein the first and second ranges of the feedback signal correspond to first and second ranges of duty cycle percentage values of a drive signal generated by the pulse width modulator circuit to switch the power switch.

6. The switching regulator of claim 2 wherein an off-time value of a drive signal generated by the pulse width modulator circuit to switch the power switch varies as a function of a level of a load coupled to the output of the power supply to vary the switching frequency of the power switch without skipping cycles for the second range of feedback signal values.

7. The switching regulator of claim 2 wherein on-time and off-time values of a drive signal generated by the pulse width modulator circuit to switch the

power switch vary simultaneously as a function of a level of a load coupled to the output of the power supply to vary the switching frequency of the power switch without skipping cycles for the second range of feedback signal values.

8. The switching regulator of claim 7 wherein the off-time value of the drive signal is varied as a function of the on-time value and a first on-time value of the drive signal, the first on-time value of the drive signal corresponding to an on-time of the drive signal at a boundary between the first and second ranges of feedback signal values.

9. The switching regulator of claim 2 wherein the switching frequency of the power switch is reduced without skipping cycles for the second range of feedback signal values as a level of load coupled to the output of the power supply is reduced.

10. The switching regulator of claim 9 wherein the switching frequency of the power switch is reduced without skipping cycles to a minimum frequency when a duty cycle percentage value of a drive signal generated by the pulse width modulator circuit to switch the power switch is substantially equal to zero percent.

11. A power supply, comprising:

an energy transfer element having an energy transfer element input and an energy transfer element output coupled to an output of the power supply;

a switching regulator circuit including a power switch coupled to the energy transfer element input, and a control circuit coupled to the power switch and the output of the power supply, the control circuit coupled to generate a feedback signal responsive to the output of the power supply, the control circuit coupled to switch the power switch in response to the feedback signal, the control circuit coupled to switch the power switch at a fixed switching frequency for a first range of feedback signal values, the control circuit coupled to vary a switching frequency of the power switch without skipping cycles in response to the feedback signal for a second range of feedback signal values.

12. The power supply of claim 11 wherein the control circuit comprises:

a feedback signal circuit coupled to the output of the power supply, the feedback signal circuit coupled to generate the feedback signal; and

a pulse width modulator circuit coupled to switch the power switch in response to the feedback signal.

13. The power supply of claim 12 further comprising an output sense circuit coupled between the output of the power supply and the switching regulator circuit, the output sense circuit coupled to provide an output sense signal to the switching regulator that is proportional to an output voltage or current supplied by the output of the power supply, wherein a duty cycle variation provided by a drive signal generated by the pulse width modulator circuit to switch the power switch is inversely proportional to the output sense signal.

14. The power supply of claim 11 wherein the first and second ranges of the feedback signal correspond to first and second ranges of levels of a load coupled to the output of the power supply.

15. The power supply of claim 12 wherein the first and second ranges of the feedback signal correspond to first and second ranges of on-time values of a drive signal generated by the pulse width modulator circuit to switch the power switch.

16. The power supply of claim 12 wherein the first and second ranges of the feedback signal correspond to first and second ranges of duty cycle percentage values of a drive signal generated by the pulse width modulator circuit to switch the power switch.

17. A method for regulating a power supply, comprising:

switching with a drive signal a power switch coupled to an energy transfer element of the power supply to control power delivered to an output of the power supply;

generating a feedback signal in response to the output of the power supply;

maintaining a frequency of the drive signal at a fixed frequency for a first range feedback signal values; and

varying the frequency of the drive signal without skipping cycles in response to the feedback signal for a second range of feedback signal values.

18. The method for regulating the power supply of claim 17 further comprising varying a duty cycle of the drive signal substantially in response to the feedback signal.

19. The method for regulating the power supply of claim 17 wherein generating the feedback signal in response to the output of the power supply comprises monitoring a current representative of a level of the load coupled to the output of the power supply.

20. The method for regulating the power supply of claim 18 wherein generating the feedback signal in response to the output of the power supply comprises monitoring an on-time of the drive signal.

21. The method for regulating the power supply of claim 20 wherein monitoring the on-time of the drive signal comprises timing the on-time of the drive signal with a timer circuit, the method further comprising suspending operation temporarily of an oscillator circuit if the on-time of the drive signal is less than a first on-time value.

22. The method for regulating the power supply of claim 21 wherein timing the on-time of the drive signal with the timer circuit comprises

discharging a capacitor at a first rate during the on-time of the drive signal; and

discharging the capacitor at a second rate during an off-time of the drive signal, the first rate greater than the second rate.

23. The method for regulating the power supply of claim 22 further comprising maintaining a voltage level of a suspended oscillating signal generated by the oscillator circuit while the operation of the oscillator circuit is temporarily suspended.

24. The method for regulating the power supply of claim 23 further comprising resuming operation of the oscillator circuit after the capacitor has been discharged.

25. A switching regulator, comprising:

a power switch coupled between first and second terminals;

a control circuit coupled to a third terminal and coupled to the power switch, the control circuit coupled to receive an output sense signal responsive to an output of a power supply, the control circuit coupled to generate a drive signal to switch the power switch in response to the output sense signal to control the output of the power supply; and

a timer circuit included in the control circuit, the timer circuit coupled to time an on-time of the drive signal, the timer coupled to the control circuit to vary a switching frequency of the drive signal without skipping cycles if the on-time of the drive signal is less than a first on-time value, the drive signal to have a fixed switching frequency if the on-time of the drive signal is greater than the first on-time value.

26. The switching regulator of claim 25 wherein the timer circuit comprises a capacitor that is coupled to be charged and discharged in response to the drive signal, the capacitor to be discharged at a first rate during the on-time of the drive signal, the capacitor coupled to be discharged at a second rate during an off-time of the drive signal, the first rate greater than the second rate.

27. The switching regulator of claim 26 wherein the timer circuit further comprises first and second current sources coupled to discharge the capacitor at the first rate, the second current source coupled to discharge the capacitor at the second rate.

28. The switching regulator of claim 26 wherein the control circuit comprises an oscillator circuit coupled to generate an oscillating signal, the oscillator circuit to suspend generating the oscillating signal if the on-time of the drive signal ends prior to the capacitor being discharged, the oscillator circuit

coupled to resume generating the oscillating signal after the capacitor has been discharged.

29. The switching regulator of claim 28 wherein the oscillator circuit is coupled to maintain a voltage level of the oscillating signal while the oscillator circuit is suspended, the oscillator circuit is coupled to resume the oscillating signal from the maintained voltage level.

ABSTRACT OF THE DISCLOSURE

A switching regulator that operates at a frequency for a first range of feedback signal values and at a variable frequency without skipping cycles for a second range of feedback signal values. In one embodiment, a switching regulator for a switched mode power supply includes a power switch coupled between drain and source terminals of the switching regulator, which are to be coupled to control the delivery of power to an output of a power supply. A control terminal of the switching regulator is to be coupled to an output of the power supply. The switching regulator includes a control circuit coupled to the control terminal and generates a feedback signal that is responsive to the output of the power supply. The control circuit also generates a drive signal that is coupled to control the switching of the power switch. The control circuit generates the drive signal responsive to the feedback signal. The drive signal has a fixed frequency for a first range of feedback signal values and at a variable frequency without skipping cycles for a second range of feedback signal values.

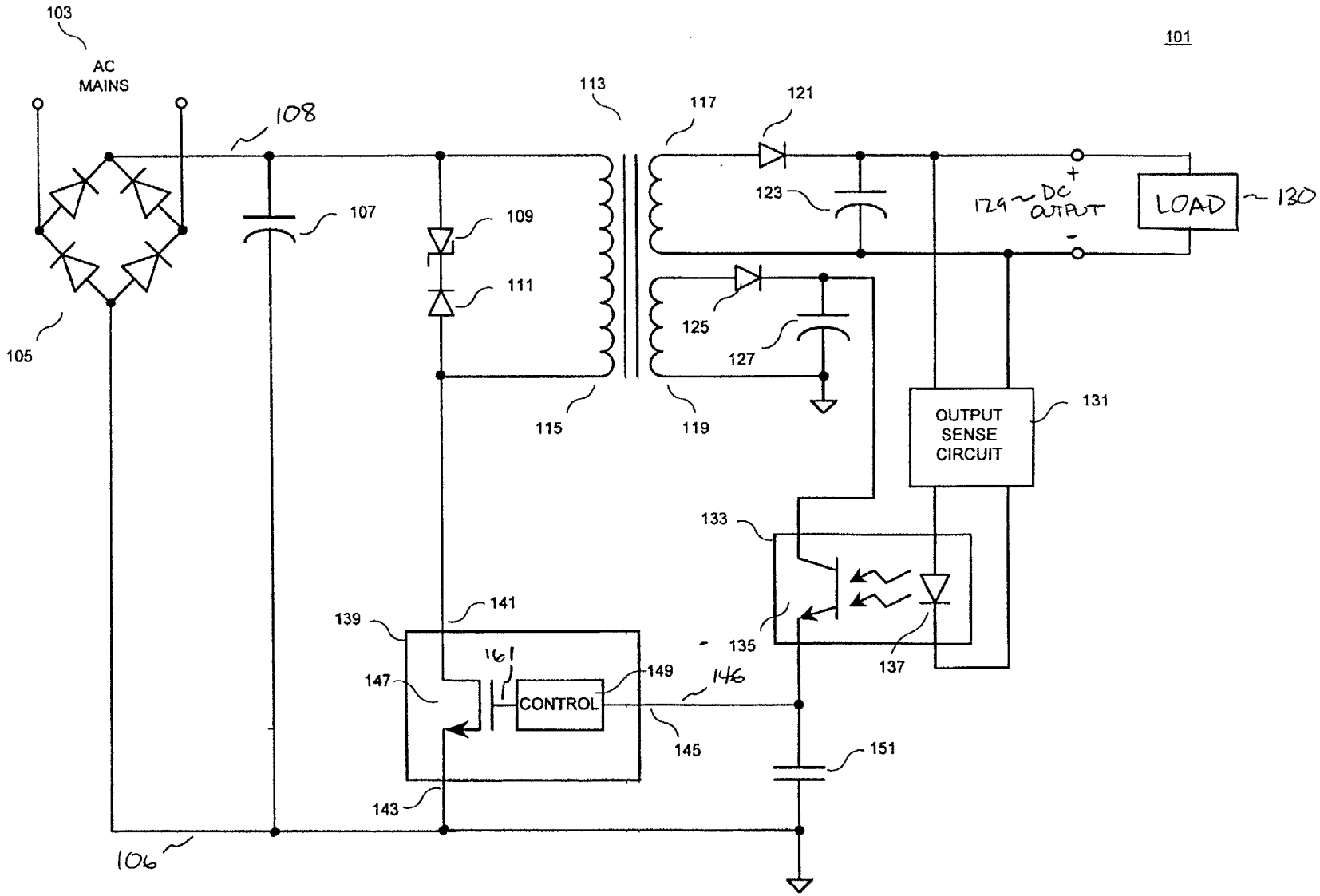


FIG. 1

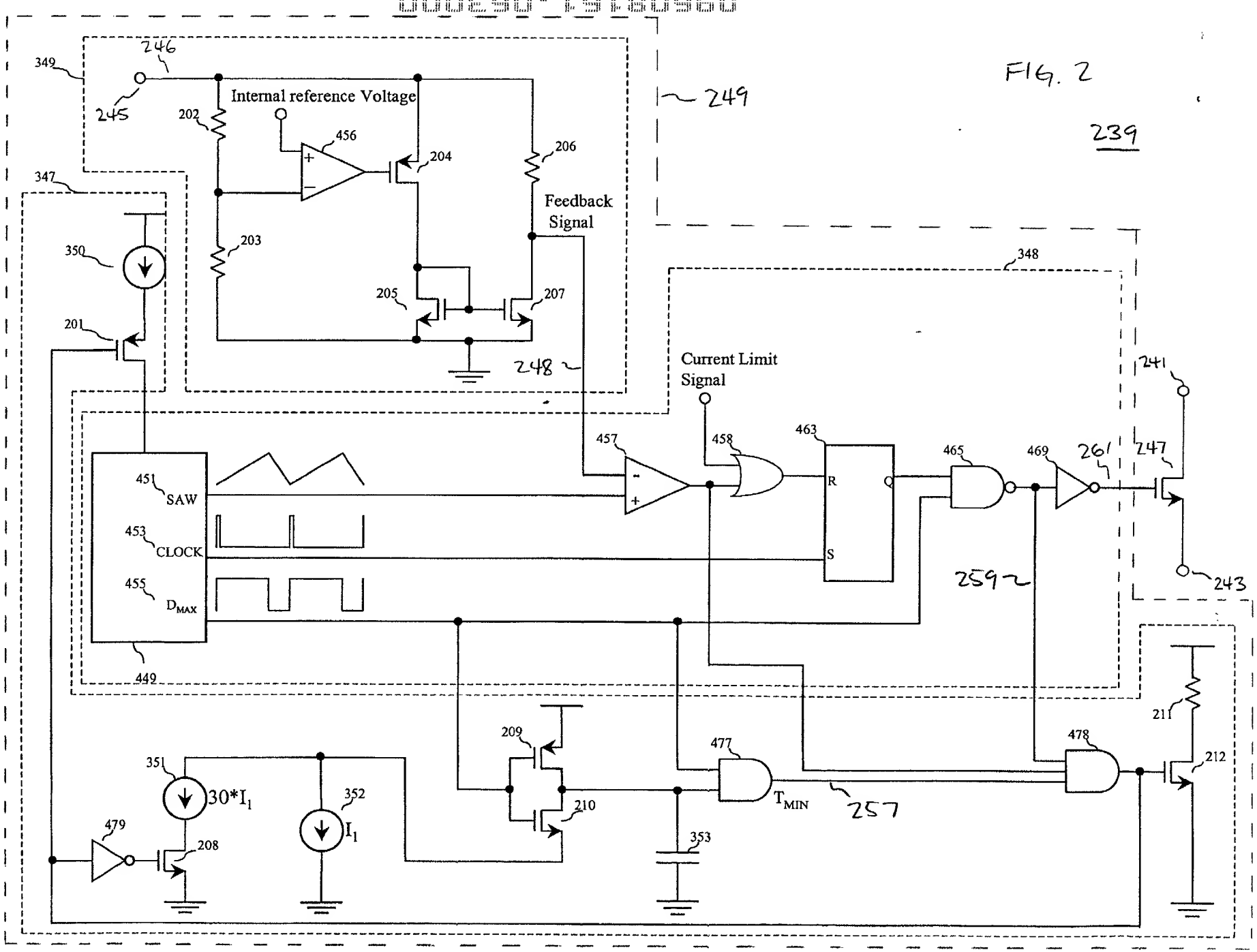


FIG. 2

FIG 3

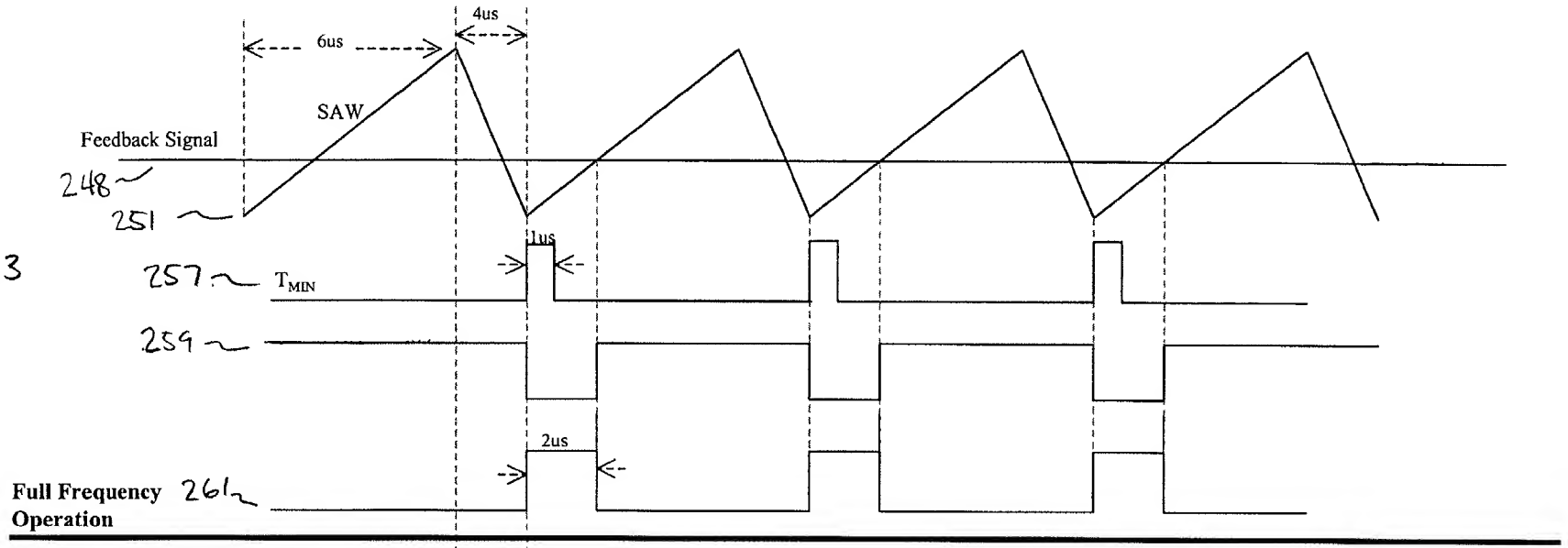


FIG 4

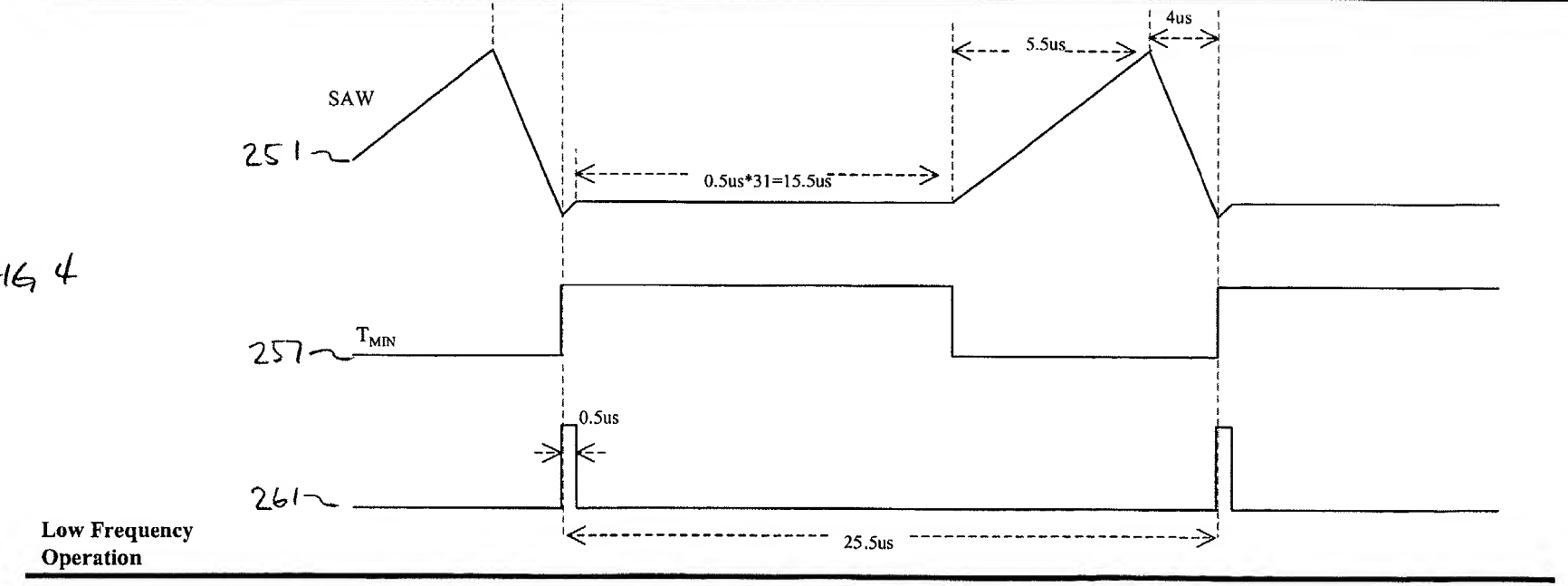


FIG. 5

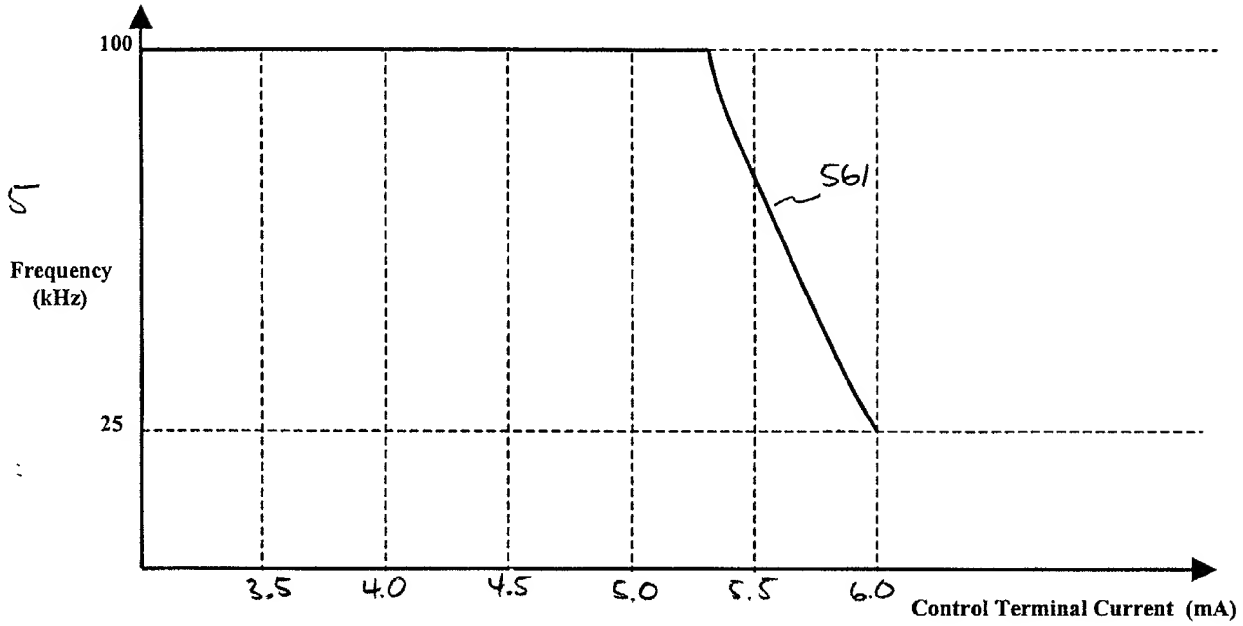
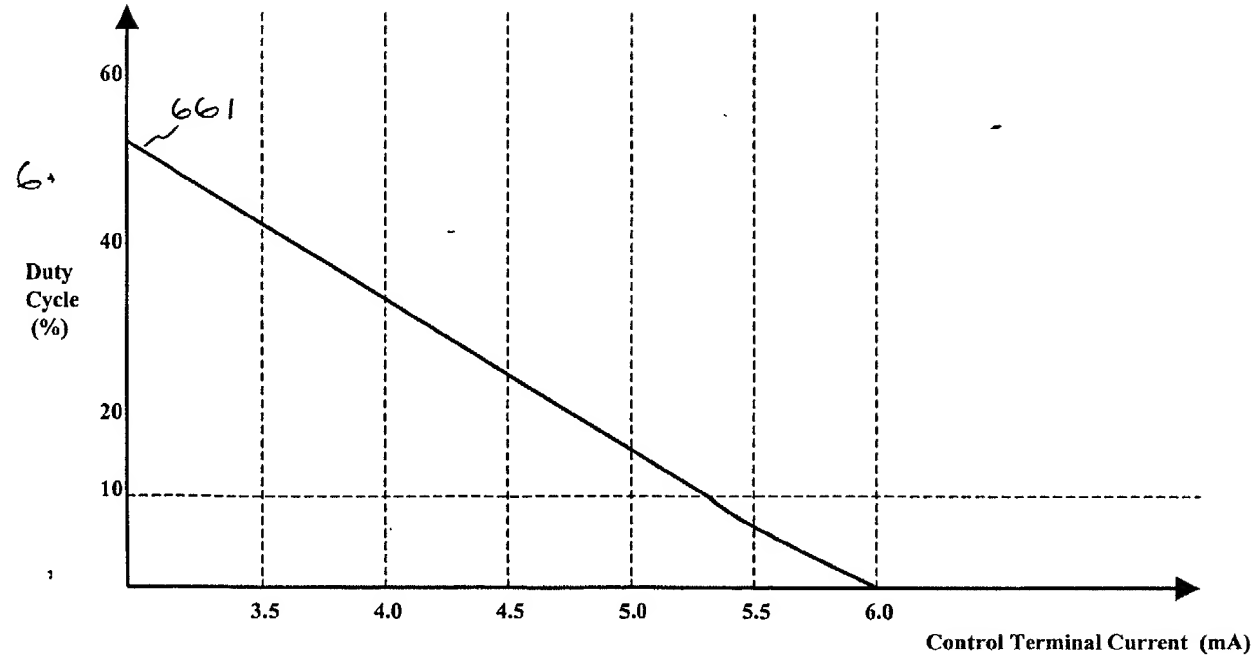

100
25
561
Frequency (kHz)
3.5
4.0
4.5
5.0
5.5
6.0
Control Terminal Current (mA)

FIG. 6


60
40
20
10
661
Duty Cycle (%)
3.5
4.0
4.5
5.0
5.5
6.0
Control Terminal Current (mA)

Attorney's Docket No.: 003692.P051 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
METHOD AND APPARATUS FOR IMPROVING EFFICIENCY IN A SWITCHING REGULATOR AT LIGHT LOADS

the specification of which

XX is attached hereto.
___ was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Day/Month/Year Filed	Yes	No
Number	Country	Day/Month/Year Filed	Yes	No
Number	Country	Day/Month/Year Filed	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status -- patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to James Y. Go (Name of Attorney or Agent), BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to James Y. Go (Name of Attorney or Agent), (425) 827-8600.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Full Name of Fourth/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____
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Full Name of Fifth/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____
_____

Full Name of Sixth/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____
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Full Name of Seventh/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____
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APPENDIX A

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APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.